

PTO-1449 (Modified) 13 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. P043D2C3C	SERIAL NUMBER 09/492,982
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE JANUARY 27, 2000	GROUP ART UNIT

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	4,945,516	07/31/90	Kashiyama	365	189.05	
	4,807,189	02/21/89	Fukushima et al.	365	220	
	4,586,167	04/21/89	Fukushima et al.	365	189.05	
	4,337,523	06/29/82	Gotta et al.	365	194	
	4,825,416	05/25/89	Tam et al.	365	194	
	4,750,839	06/14/88	Wang et al.	365	233	
	4,513,370	04/23/85	Ziv et al.	709	253	
	4,099,231	07/04/78	Kotok et al.	711	168	
TNT	5,175,835	12/29/92	Beighe et al.	711	212	

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

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TNT	4,891,791	01/02/90	Iijima	365	189.01	
	4,092,665	05/30/78	Saran	341	63	
	5,093,807	03/03/92	Hashimoto et al.	365	230.09	
	3,882,470	05/06/75	Bunter	365	200	
	5,083,296	01/21/92	Tara et al.	365	230.02	
	4,792,926	12/20/88	Roberts	365	189.02	
	4,719,602	01/12/88	Hag et al.	365	189.02	
	4,785,394	11,15,88	Fischer	710	114	
	5,083,260	01/21/92	Tsuchiya	710	113	
	4,954,987	09/04/90	Auvinen et al.	365	189.02	
	4,675,850	06/23/87	Kumanoya et al.	365	189.08	
TNT	4,788,667	11/29/88	Nakano et al.	365	193	

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TNT	M. Bazes et. al., "A Programmable NMOS DRAM Controller for Microcomputer Systems with Dual-Port Memory and Error Checking and Correction", IEEE Journal of Solid State Circuits, vol. 18 No. 2, pp. 164-172 (Apr. 1983)
TNT	A. Agarwal, "An Evaluation of Directory Schemes for Cache Coherence", IEEE document pp.280-289 (1988)
TNT	D. Kawley, "SUPERFAST BUS SUPPORTS SUPERFAST TRANSACTIONS", High Performance Systems, pp 90-94 (Sept. 89)
TNT	H. L. Kalter et al. "A 50-ns 16Mb DRAM with a 10-ns Data Rate and On-Chip ECC", IEEE Journal of Solid State Circuits, vol. 25 No. 5, pp. 1118-1128 (Oct 1990)
TNT	S. Watanabe et. al., "AN Experimental 16-Mbit CMOS DRAM Chip with a 100-MHz Serial READ/WRITE Mode", IEEE Journal of Solid State Circuits, vol. 24 No. 3, pp. 763-770 (June 1982)

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TNT	4,445,204	04/24/84	Nishiguchi	365	194	
	4,821,226	04/11/89	Christopher et al.	365	230.03	
	4,882,712	11/21/89	Ohno et. al.	365	206	
	4,951,251	08/21/90	Yamaguchi et al.	365	189-02	
	4,928,265	12/29/92	Beighe et al.	365	189-01	
	5,107,465	04/21/92	Fung et al.	365	230-08	
	5,206,833	04/27/93	Lee	365	233	
	4,953,128	08/28/90	Kawai et al.	365	194	

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TNT	L. R. Metzger, "A 16K CMOS PROM with Polysilicon Fusible Links", IEEE Journal of Solid State Circuits, vol. 18 No. 5, pp. 562-567 (Oct. 1983)
TNT	A. Yuen et. al., "A 32K ASIC Synchronous RAM Using a Two-Transistor Basic Cell", IEEE Journal of Solid State Circuits, vol. 24 No. 1, pp. 57-61 (Feb. 1989)
TNT	D.T. Wong et. al., "An 11-ns 8Kx18 CMOS Static RAM with 0.5-μm Devices", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1095-1103 (Oct. 1988)
TNT	T. Williams et. al., "An Experimental 1-Mbit CMOS SRAM with Configurable Organization and Operation", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1085-1094 (Oct. 1988)

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TNT	5,140,688	08/18/92	White et al.	395	550	
/	5,018,111	05/21/91	Madland	365	233	
	4,734,880	03/29/88	Collins	74	605	
	4,183,095	01/08/80	Ward	365	689.02	
	4,975,872	12/04/90	Zaiki	365	49	
	5,016,226	05/14/91	Hiwada et al.	365	233	
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TNT	F. Miller et. al., "HIGH FREQUENCY SYSTEM OPERATION USING SYNCHRONOUS SRAMS", Midcon/87 Conference Record, pp. 430-432 Chicago, IL, USA; 15-17 Sept. 1987
TNT	K. Ohta, "A 1-Mbit DRAM with 33-MHz Serial I/O Ports", IEEE Journal of Solid State Circuits, vol. 21 No. 5, pp. 649-654 (Oct. 1986)
TNT	K. Nogami et. al., "A 9-ns HIT-Delay 32-kbyte Cache Macro for High-Speed RISC", IEEE Journal of Solid State Circuits, vol. 25 No. 1, pp. 100-108 (Feb. 1990)
TNT	F. Towler et. al., "A 128k 6.5ns Access/ 5ns Cycle CMOS ECL Static RAM", 1989 IEEE international Solid State Circuits Conference, (Feb. 1989)
TNT	M. Kimoto, "A 1.4ns/64kb RAM with 85ps/3680 Logic Gate Array", 1989 IEEE Custom Integrated Circuits Conference

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TNT	4,799,199	01/17/89	Scales, III et al.	365	230.08	
	5,142,637	09/25/92	Harlin et al.	345	425	
	5,148,523	09/15/92	Harlin et al.	345	519	
	4,954,987	09/04/90	Luvinen et al.	365	189.02	
	4,675,850	06/23/87	Nakano et al.	365	230.01	
	4,788,667	05/22/90	Higuchi	365	193	
	4,937,734	06/26/90	Bechtolsheim	711	202	
	4,680,738	07/14/87	Tam	365	239	
	4,845,664	07/04/89	Aichelmann, Jr. et al.	364	900	
TNT	4,920,483	04/24/90	Pogue et al.	364	200	

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TNT	D. Wendell et. al. "A 3.5ns, 2Kx9 Self Timed SRAM", 1990 IEEE Symposium on VLSI Circuits (Feb 1990)
TNT	M. Bazes et. al., "A Programmable NMOS DRAM Controller for Microcomputer Systems with Dual-Port Memory and Error Checking and Correction", IEEE Journal of Solid State Circuits, vol. 18 No. 2, pp. 164-172 (Apr. 1983)
TNT	R. Schmidt, "A memory Control Chip fo Formatting Data into Blocks Suitable for Video Applications", IEEE Transactions on Circuits and Systems, vol. 36, No. 10 (Oct. 1989)
TNT	D. K. Morgan "The CVAX CMCTL - A CMOS Memory Controller Chip", Digital Technical Journal, No. 7 (Aug. 1988)
TNT	T.C. Poon et. al., "A CMOS DRAM-Controller Chip Implementation", IEEE Journal of Solid State Circuits, vol. 22 No. 3, pp. 491-494 (June 1987)
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TNT	E.H. Frank "The SBUS: Sun's High Performance System Bus for RISC Workstations" Sun Microsystems Inc. 1990

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